The Transmission-Line High-Efficiency Class-E Amplifier

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Abstract—**High-efficiency switched-mode (heavily saturated) circuits such as the class-E amplifier are well-known in the MHz frequency range. Here, a microwave transmission-line class-E amplifier is presented. Design equations for the output circuit line lengths and impedances are derived, along with approximate equations predicting power and efficiency for the class-E amplifier. Microstrip circuits using the Siemens CLY5 MESFET demonstrate 80% power-added efficiency (PAE) at 0.5 GHz with 0.55 W of output power and 73% PAE at 1.0 GHz with 0.94 W. Experimental results compare favorably to a simplified design-oriented analysis.**

I. Introduction

THE TRANSMISSION-LINE class-E switched-mode amplifier topology is shown in Fig. 1. The capacitance C_s is the transistor's output capacitance, which acts as an integral part of the circuit. An ideal switch converts dc power to microwave power in the class-E circuit without losses. In practice, finite resistance present in a transistor (such as a MESFET's ON-resistance) limits the maximum efficiency of operation. At low MHz frequencies, such circuits exhibit efficiencies as high as 96% using lumped elements [1]. The class-E concept can also be extended to high-efficiency multiplier operation [2]. To date, microwave amplifiers utilizing harmonic termination concepts have made use of the class-F concept [3], [4].

II. Transmission-Line Class-E Analysis

In the circuit shown in Fig. 1, the voltage at the gate of the transistor is assumed to be a large sinusoid. During the upper half of the sinusoid at the gate, the transistor is assumed to be turned "ON," and during the lower half of the sinusoid the transistor is assumed to be in its "OFF"-state. To simplify the analysis of the class-E circuit, the current flowing into the switched capacitor is assumed to be sinusoidal (the voltage across the switch is *not* sinusoidal) [5]. From this assumption, and from the boundary conditions imposed upon the switch voltage [1], it is found that the harmonic termination for the transistor output port should be an open-circuit for all harmonic frequencies to give class-E operation. At the fundamental frequency of operation, the impedance of the load network attached to the switched capacitor is found to be

Manuscript received March 6, 1995. This work was supported by Compact Software under Phase I of an STTR with the U.S Air Force and by NSF under a Presidential Faculty Fellow Award.

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IEEE Log Number 9413481.

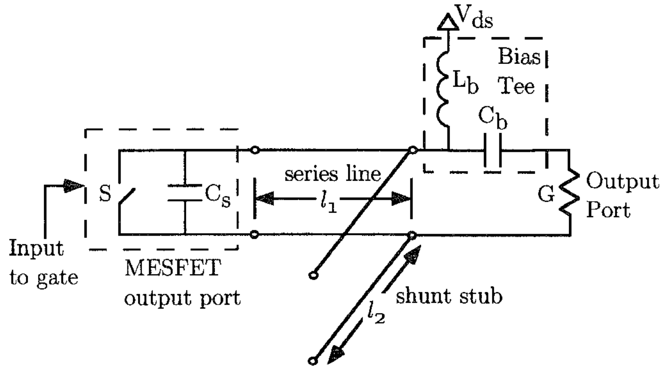

Fig. 1. The transmission-line class-E circuit. Transmission lines l_1 and l_2 are assumed to be between 0 and 90° long.

$$Z_{\text{net}_1} = \frac{\kappa_0}{\omega_s C_s} e^{j\theta_0} \simeq \frac{0.28015}{\omega_s C_s} e^{j49.0524^\circ}. \quad (1)$$

The constants κ_0 and θ_0, and all of the equations presented in this paper, are derived in [6]. In practice, simulations and experiments have shown that an open-circuit termination at the second harmonic is sufficient to produce approximate class-E operation. For the topology shown in Fig. 1, the lengths l_1 and l_2 may be set to 45° to ensure open-circuit termination at the second harmonic. Then, their characteristic impedances can be adjusted for the correct fundamental impedance Z_{net_1}. Applying standard transmission-line formulas to the topology shown, two equations are found relating the transmission line lengths and characteristic admittances

$$\omega_s C_s \cos\theta_0((Y_1 - AB)^2 + (AG)^2) - \kappa_0 Y_1(G(Y_1 - AB) + AG(B + AY_1)) = 0 \quad (2)$$

$$\omega_s C_s \sin\theta_0((Y_1 - AB)^2 + (AG)^2) + \kappa_0 Y_1((B + AY_1)(Y_1 - AB) - AG^2) = 0 \quad (3)$$

where $A = \tan\beta_1 l_1$ and $B = Y_2 \tan\beta_2 l_2$. The constants κ_0 and θ_0 are defined in (1), and Y_1 and Y_2 are the characteristic admittances of lines l_1 and l_2. The output port has a conductance G.

The transistor's ON-state resistance is the primary source of loss in the transmission-line class-E circuit. During the ON-state, the transistor is assumed to be a constant resistance R_s.

TABLE I
COMPARISON OF THEORY AND EXPERIMENT FOR THE TRANSMISSION-LINE CLASS-E AMPLIFIER AT 0.5, 1, AND 2 GHz

Frequency	0.5 GHz	1.0 GHz	2.0 GHz
$Gain_{meas}$	15.3 dB	14.7 dB	9.1 dB
PAE_{meas}	80 %	73 %	54 %
$\eta_{d\ pred}$	85 %	73 %	56 %
$\eta_{d\ meas}$	83 %	75 %	62 %
$P_{out\ pred}$	0.77 W	1.35 W	2.07 W
$P_{out\ meas}$	0.55 W	0.94 W	0.53 W

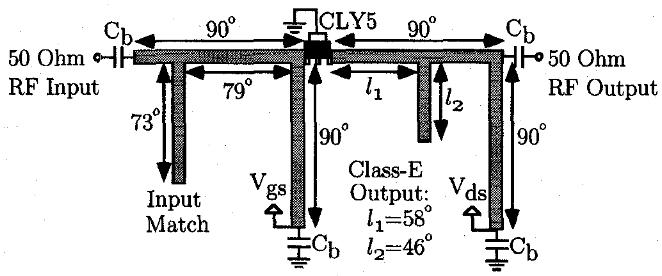

Fig. 2. Class-E microstrip amplifier at 0.5 GHz.

During its OFF-state, it is assumed to be a constant capacitance C_s as before. Under these assumptions, an approximate expression for drain efficiency is found

$$\eta_d = \frac{1 + \left(\frac{\pi}{2} + \omega_s C_s R_s\right)^2}{\left(1 + \frac{\pi^2}{4}\right)(1 + \pi\omega_s C_s R_s)^2}. \quad (4)$$

For the Siemens CLY5 MESFET considered in the next section, estimated values of $C_s = 2.6$ pF and $R_s = 4\ \Omega$ are assumed for large-signal sinusoidal gate-source excitation. The dc power and output power of the class-E circuit are given by

$$P_{\rm dc} = \pi\omega_s C_s V_g^2 \quad \text{and} \quad P_{\rm out} = \eta_d P_{\rm dc}. \quad (5)$$

An approximate maximum frequency of class-E operation for a given transistor can also be found from

$$f_{\max} \simeq \frac{I_{\max}}{56.5 C_s V_{ds}} \quad (6)$$

where $I_{\max}$ is the peak output current for the transistor (slightly larger than I_{dss} for a MESFET). An approximation to class-E operation is possible above this frequency limit [7], and such a circuit is demonstrated experimentally in the next section.

III. EXPERIMENTAL RESULTS AT 0.5, 1, AND 2 GHz

Class-E circuits using the Siemens CLY5 MESFET (5 mm gate width) and the above transmission-line topology were designed, fabricated and tested at 0.5, 1, and 2 GHz. All three circuits used the same microstrip circuit topology. Experimental results are compared to the above approximate formulas in Table I. All three circuits were operated at the same bias point, with $V_{ds} = 6.0$ V and $V_{gs} = -2.4$ V.

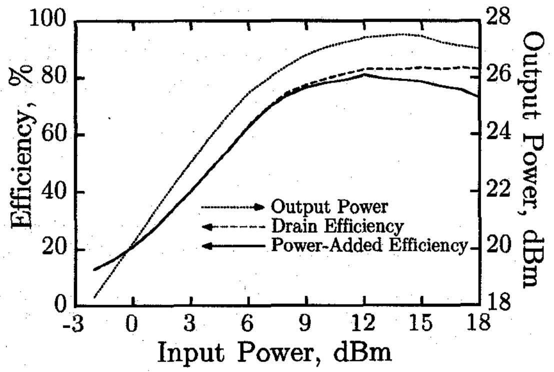

Fig. 3. Output power and efficiency as a function of input power level for the 0.5-GHz microstrip class-E amplifier.

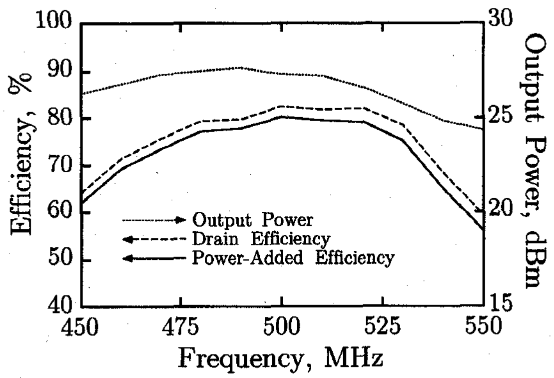

Fig. 4. Output power and efficiency as a function of frequency for the 0.5-GHz microstrip class-E amplifier. The input power is 12 dBm.

For the Siemens CLY5, the maximum frequency of ideal class-E operation is approximately 1.4 GHz at a supply voltage of 6 V. The 2-GHz class-E circuit demands a higher peak drain current than the MESFET can provide. This explains why the output power level is much lower than expected at this frequency (see Table I). At the upper frequency limit for a given transistor, the class-E approximation breaks down and more traditional (class-A, class-AB) amplifier design concepts become more appropriate, since the transistor can only generate fundamental (sinusoidal) signals at these frequencies.

The 0.5-GHz circuit is shown in Fig. 2. The microstrip lines are all 50 Ω, and the substrate is 2.54-mm-thick Duroid, with $\epsilon_r = 10.5$. The output power, drain efficiency, and power-added efficiency are plotted as a function of input power level in Fig. 3, and as a function of frequency in Fig. 4. The power-added efficiency remains above 75% over a 10% bandwidth, and it remains above 50% over a 26% bandwidth.

The 0.5-GHz class-E circuit was designed assuming $C_s = C_{ds} = 2.4$ pF from a nonlinear Materka model for the MESFET provided by Compact Software. From experimental adjustment of the 0.5-GHz class-E output circuit for maximum efficiency, it was found that the capacitor C_s was 2.6 pF, and a drain lead inductance of 1.7 nH was needed between the switched capacitor and the series transmission line in Fig. 1. *The 1- and 2-GHz class-E output circuits were designed and measured according to the above equations without experimental adjustment.*

ACKNOWLEDGMENT

The authors would like to thank Dr. R. Tayrani of Compact Software for many helpful discussions, as well as for providing devices and a nonlinear Materka model.

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